REMARKS/ARGUMENTS

Claims 10 through 16 and 22 through 29 and 30 to 32 remain in the application. Claims 10 through 13, 16 and claim 30 have been amended. Claim 30 as now amended is in independent form, incorporating the limitations of amended claim 10. The Applicant would like to thank the Examiner for his diligent examination.

The title has been amended and is submitted herewith in Attachment A to be indicative of the invention to which the claims are directed. The title has been amended to read "SI-GE Base Heterojunction Bipolar Device."

The Abstract has been amended to describe a semiconductor device rather than a method of manufacture and is submitted herewith in Attachment A.

Informalities on page 15, lines 12 and 15, have been corrected as submitted herewith in paragraph 0063 in Attachment A. Due to a clerical error at the time of filing, paragraphs 0040, 0041 and 0042 in the Brief Description of the Drawings and paragraphs 0052, 0053 and 0062 in the Detailed Description did not correspond to the labeling of Figures 3a, 3b and 3c. Applicant has taken this opportunity to amend paragraphs 0040, 0041, 0042, 0052, 0053 and 0062 to now correspond to the labeling of Figures 3a, 3b and 3c. No new matter has been added.

Figures 5 through 13 have been amended to include reference numerals present in some of the figures, but not all. With respect to Figure 13, a number "2" was inadvertently included in the Figure, next to the "B", and this has been removed. No new matter has been included in the amended figures.

Claim Rejection Under 35 U.S.C. 102

Claims 10-16 and 22-29 have been rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki U.S. Patent No. 5,955,745 ('745).

Applicant would like to direct the Examiner's attention to the Figures 6a through 7b of '745. From these figures and supporting text in the specification it is evident to one of skill in the art that these processes are for producing of a field effect transistor device (MOSFET) and not a bipolar junction transistor device (BJT) as has been claimed and disclosed. Wither reference to Figures 6a through 7b and supporting text in the specification, the formation of a collector and an emitter terminal is not disclosed.

Referring to claim 10, the applicant discloses the use of a layer of polysilicon for forming of the BJT. With reference to Figures 6a through 7b of '745, single crystal silicon is used and not polysilicon. The Examiner will note upon review of the affidavit of S. Kovacic submitted herewith, in addition to common knowledge of those of skill in the art, that FET devices cannot use polysilicon because electrons do not propagate well in an electrical channel formed in polysilicon. Thus, one of skill in the art would not refer to Figures 6a through 7b of '745, as well as supporting text found in the specification, to utilize such information in manufacturing of the Bi-polar device as claimed.

Figures 12 and 13 of '745 on the other hand, disclose the formation of a transistor that is other than a field effect transistor. The text in '745 supporting these figures discloses the formation of an emitter terminal.

With reference to FIG. 12b and 12c of '745, it is disclosed in '745 (starting at Col 10, line 64), that: "After SiGe spacer layer 27 and P-type Si base layer (silicon intrinsic base layer) 28 are formed, P-type polycrystalline silicon layer 29 of 100 to 300 nm containing boron and an inter-layer insulating film, for example, oxide film 30, of 100 to 300 nm thick are successively formed over the entire area as seen in FIG. 12(c). Then, they are patterned into base leading out electrode 29a of a predetermined shape, and side wall insulating film 31, of for example, 100 to 300 nm thick of a nitride film is formed by a known technique on an end face of base leading out electrode 29a."

As evidenced by the affidavit of S. Kovacic submitted herewith, it is obvious to one of skill in the art that in order to achieve a window region within the "P-type polycrystalline silicon layer 29," a step of etching of the polycrystalline silicon is required before the emitter electrode 32a can be disposed therein for contacting the silicon layer 28. The etching of this polycrystalline silicon layer 29 takes place in a time dependent etching process, which results in removal of a portion of the underlying silicon layer 28. The underlying silicon layer 28 does not act as an etch stop for removal of the polycrystalline silicon layer, since the material difference between these two layers is not distinguishable to the etchant.

Unfortunately, though it is known to perform etching to form the window in the polycrystalline silicon layer 29, as evidenced by the affidavit of S. Kovacic submitted herewith, all attempts to do so have resulted in poor or non-uniform devices since the resultant etching is not truly uniform (on the scale of integrated circuit manufacture) across the entire wafer and each transistor is left having different electrical characteristics. Furthermore, the etching of the window region results in a deeper etched centre portion of the window than at the edges of the window, also resulting in undesirable characteristics of the manufactured transistor devices. In the present specification at page 12 and relating to an embodiment of the invention the applicant discloses that: "It is important that the SiGe/Si layers 112 and 114 not be inadvertently etched since the p-type dopant is already positioned within the layer 112 grown on the silicon substrate 110; this is in contrast to prior art techniques where an ion implanter is used to dope the base region of the transistor with p-type dopant. Thus, if some of the SiGe/Si layers were inadvertently etched, the overall thickness and/or the uniformity of the thickness of the SiGe layer will be varied, altering the transistor's electrical characteristics. Of course it is desired to have uniformity across the transistor base layer."

The Examiner will note upon review of the affidavit of S. Kovacic as submitted herewith, that when a transistor device is manufactured using the processes of '745, this results in transistor devices that do not have performance characteristics nearly identical from one

part to another manufactured on a same wafer. Thus, the Beta resulting from the formation of this type of transistor is variable across a batch of transistors manufactured on a same wafer using this process. Furthermore, attaining a same beta for the majority of these transistors is difficult or impossible because of the removal of a portion of the underlying silicon layer as a result of the etching process used for forming a window in the adjacent polysilicon layer 29. To those of skill in the art it is known that the formation of a transistor device results when '745 is used, however each transistor formed has different characteristics and thus yield of the devices is not predictable nor optimal.

In an embodiment, the applicant uses a Si3N4 plug disposed on the silicon layer prior to oxidation thereof, thereafter an etching process is used that removes this plug in a repeatable manner without affecting underlying silicon layer (Si3N4 being substantially different from the underlying silicon layer). Thus, the process as taught by the applicant yields a repeatable thickness silicon layer after removal of the Si3N4, which results in a more predictable device yield. Using an etching process incompatible with etching of the silicon layer ensures that the transistor's electrical characteristics are repeatably manufacturable, as evidenced by the affidavit of S. Kovacic submitted herewith.

Applicant would also like to note that the region denoted by numeral 33 as illustrated in '745 FIG. 12d is a diffusion region. Referring to Figure 13, Applicant denotes a similar region with a dashed line extension of the n+ emitter terminal. Applicant notes that this dashed line illustrated in Figure 13 does not indicate a diffusion region. Furthermore, referring to figures 12a through 12e of '745, the etching of the underlying silicon layer is not illustrated because the figures of '745 as provided are idealized drawings. Further, it is difficult to quantify the etching of the underlying silicon for the purposes of drawings because each transistor may have substantially different amounts of material removed therefrom. As evidenced by the affidavit of S. Kovacic submitted herewith, it would be impossible to etch the overlaid silicon material completely without removing some of the underlying material absent an etch stop layer.

Claim 10 as amended recites the limitation "the layer of SiGe having its surface unaffected by a process of etching within the window region, the first layer of polysilicon forming a base terminal of the transistor; and, a second layer of polysilicon of the first conductivity type covering and contacting the unetched SiGe layer of the transistor, said layer of polysilicon forming the other of the collector and the emitter." With the amendment made to claim 10 and in view of the aforementioned arguments, claim 10 is not anticipated by '745. Claims 11 and 12 are dependent from an allowable claim and are thus allowable.

Claim 13 has been amended to recite the following limitation, "a second layer of silicon of the first conductivity type covering the window region and contacting the SiGe layer within this small window, where the SiGe layer within the window region has a surface unaffected by a process of etching." With the amendment made to claim 13 and in view of the aforementioned arguments, claim 13 is not anticipated by '745. Claims 10 through 16, and 22 through 29 are dependent from an allowable claim and are thus allowable.

Applicant respectfully submits that claims 14 through 16, and 22 through 29 are now allowable.

Claim Rejection Under 35 U.S.C. 112

Claims 30-32 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to claim 30, it has been redrafted to be in an independent form, which includes the limitations of amended claim 10 and includes the further limitation of: "wherein the SiGe layer has a controllable thickness profile in a direction transverse the layers within the semiconductor substrate within predetermined limits, the controllable thickness profile for providing substantially reproducible results for the thickness of the SiGe layer." The claim, with limitations as filed, is believed to be clear and allowable. In

particular, the terms "controllable" and "reproducible" are terms easily understood by those of skill in the art. In particular, prior art attempts at forming double poly SiGe bipolar junction transistors result in non-reproducible transistor formation due to a lack of precise control over an etching process and therefore a lack of control over the thickness, as is the case in '745. The "thickness" referred to is understood by those of skill in the art as a thickness of the layer – in a direction perpendicular to a plane of a surface of the wafer on which the layer is deposited. That said, the term thickness is now clearly defined within the specification in amended paragraph 0062.

Claims 31 and 32 depend from claim 30, which is now in allowable form.

No new matter has been added in the amended claims.

Applicant looks forward to favourable reconsideration of the present application.

Please charge any additional fees required or credit any overpayment to Deposit Account No: 50-1142.

Respectfully,

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#9 Misc Letter
YRobinson
4/24/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application Of: Kovacic et al. No: 115-01 US DIV(2)

Application No.: 09/988,938 Group Art: 2823

Filing Date: February 1, 2002 Examiner: Pham, Thanh V

Title: Method of Producing a SI-GE Base Heterojunction Bipolar Device

March 27, 2003

The Commissioner Of Patents And Trademarks
Washington, D.C., 20231, U.S.A.

AFFIDAVIT UNDER 37 C.F.R. 1.132

Sir:

I, Steven J. Kovacic, am the inventor in the above-captioned application. I have thoroughly reviewed the Office Action in the above-captioned application dated February 1, 2002. My analysis of the Office Action and the cited United States Patent No. 5,955,745 ('745) is as follows.

Regarding Figures 6a through 7b of '745, it is evident to one of skill in the art that these processes are for producing of a field effect transistor device (MOSFET) and not a bipolar junction transistor device (BJT) as has been claimed and disclosed. Wither reference to Figures 6a through 7b and supporting text in the specification, the formation of a collector and an emitter terminal is not disclosed.

Referring to claim 10, the use of a layer of polysilicon for forming of the BJT is disclosed. With reference to Figures 6a through 7b of '745, single crystal silicon is used and not polysilicon. To those of skill in the art it is known that FET devices cannot use polysilicon because electrons do not propagate well in an electrical channel formed in polysilicon. Thus, one of skill in the art would not refer to Figures 6a through 7b of '745, as well as supporting text found in the specification, to utilize such information in manufacturing of the Bi-polar device as claimed.

Figures 12 and 13 of '745 on the other hand, disclose the formation of a transistor that is other than a field effect transistor. The text in '745 supporting these figures discloses the formation of an emitter terminal.

With reference to FIG. 12b and 12c of '745, it is disclosed in '745 (starting at Col 10, line 64), that: "After SiGe spacer layer 27 and P-type Si base layer (silicon intrinsic base layer) 28 are formed, P-type polycrystalline silicon layer 29 of 100 to 300 nm containing boron and an inter-layer insulating film, for example, oxide film 30, of 100 to 300 nm thick are successively formed over the entire area as seen in FIG. 12(c). Then, they are patterned into base leading out electrode 29a of a predetermined shape, and side wall insulating film 31, of for example, 100 to 300 nm thick of a nitride film is formed by a known technique on an end face of base leading out electrode 29a."

It is obvious to one of skill in the art that in order to achieve a window region within the "P-type polycrystalline silicon layer 29," a step of etching of the polycrystalline silicon is required before the emitter electrode 32a can be disposed therein for contacting the silicon layer 28. The etching of this polycrystalline silicon layer 29 takes place in a time dependent etching process, which results in removal of a portion of the underlying silicon layer 28. The underlying silicon layer 28 does not act as an etch stop for removal of the polycrystalline silicon layer, since the material difference between these two layers is not distinguishable to the etchant.

Unfortunately, though it is known to perform etching to form the window in the polycrystalline silicon layer 29, all attempts to do so have resulted in poor or non-uniform devices since the resultant etching is not truly uniform (on the scale of integrated circuit manufacture) across the entire wafer and each transistor is left having different electrical characteristics. Furthermore, the etching of the window region results in a deeper etched centre portion of the window than at the edges of the window, also resulting in undesirable characteristics of the manufactured transistor devices.

It is important that the SiGe/Si layer not be inadvertently etched differently or non-uniformly since the p-type dopant is already positioned within the layer grown on the silicon substrate. Thus, when a transistor device is manufactured using the processes of '745, this results in transistor devices that do not have repeatable performance characteristics. Thus, the Beta resulting from the formation of this type of transistor is variable across a batch of transistors manufactured on a same wafer using this process. Furthermore, attaining a same beta for the majority of these transistors is difficult or impossible because of the removal of a portion of the underlying silicon layer as a result of the etching process used for forming a window in the adjacent polysilicon layer 29. To those of skill in the art it is known that the formation of a transistor device results when '745 is used, however each transistor formed has different characteristics and thus yield of the devices is not predictable.

In patent application 09/988,938, a method of forming a double polysilicon BJ transistor (BJT) is disclosed allowing for controlled etching to form the window region. I am unaware of any method for forming the window region absent etching of the underlying silicon layer that predate the date of application of the above noted patent application 09/988,938. The process as taught supports a repeatably manufacturable transistor device.

I respectfully request that the Examiner reconsiders the outstanding rejection in light of the above declaration.

Respectfully submitted,

Date: Mar. 25, 2003

Stephen J. Kovacic